REMARKS

This is in full and timely response to the Office Action dated February 22, 2008.

Claims 14 and 16-25 are currently pending in this application, with claims 14 and 16 being independent.

No new matter has been added.

Reexamination in light of the following remarks is respectfully requested.

Entry of amendment

This amendment *prima facie* places the case in condition for allowance. Alternatively, it places this case in better condition for appeal.

Accordingly, entry of this amendment is respectfully requested.

Prematureness

Applicant, seeking review of the *prematureness* of the final rejection within the Final Office Action, respectfully requests reconsideration of the finality of the Final Office Action for the reasons set forth hereinbelow. See M.P.E.P. §706.07(c).

Claim objection

While not conceding the propriety of the claim objection found within paragraph 2 of the Office Action and in order to advance the prosecution of the above-identified application, claim 9 has been canceled and claim 14 amended.

Appreciation is expressed for the Examiner's helpful suggestion.

Rejections under 35 U.S.C. §103

Paragraph 4 of the Office Action indicates a rejection of claims 9-13 under 35 U.S.C. §103 as allegedly being unpatentable over U.S. Patent No. 6,307,227 (Fujii) in view of U.S. Patent No. 5,013,677 (Hozumi), and further in view of U.S. Patent No. 6,885,081 (Morimoto).

Paragraph 11 of the Office Action indicates a rejection of claims 14-15 under 35 U.S.C. §103 as allegedly being unpatentable over U.S. Patent No. 6,307,227 (Fujii) in view of U.S. Patent No. 5,013,677 (Hozumi), and further in view of U.S. Patent No. 6,885,081 (Morimoto), and further in view of U.S. Patent Application Publication No. 2003/0235984 (Besser).

These rejections are traversed at least for the following reasons.

Claims 9-13 and 15 - While not conceding the propriety of these rejections and in order to advance the prosecution of the above-identified application, claims 9-13 and 15 have been canceled.

Claim 14 - Claim 14 has been placed into independent form. Claim 14 is drawn to a method for manufacturing a bipolar transistor, the method comprising the steps of:

> forming a base layer (18) on an insulator, said base layer (18) being in contact with a portion of a semiconductor substrate;

forming an insulating film (2) on said base layer (18);

forming base and emitter electrode lead openings (4, 5) within said insulating film (2), said base electrode lead opening (5) being formed simultaneous with said emitter electrode lead opening (4);

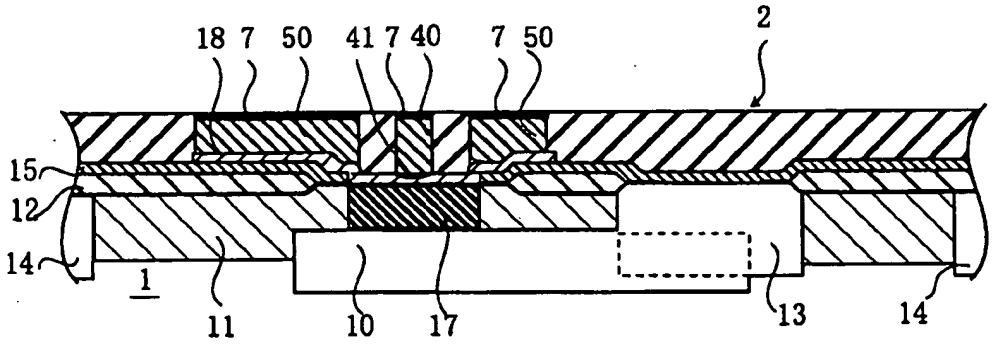
depositing a conducting film (6) into said base electrode lead opening (5) and into said emitter electrode lead opening (4), said conducting film (6) within said base electrode lead opening (5) being a base electrode lead portion (50) and said conducting film (6) within said emitter electrode lead opening (4) being an emitter electrode lead portion (40); thereafter,

polishing said conducting film (40, 50) to separate said base electrode lead portion (50) from said emitter electrode lead portion (40); and

depositing a silicide (7) onto a polished surface of said conducting film (40, 50).

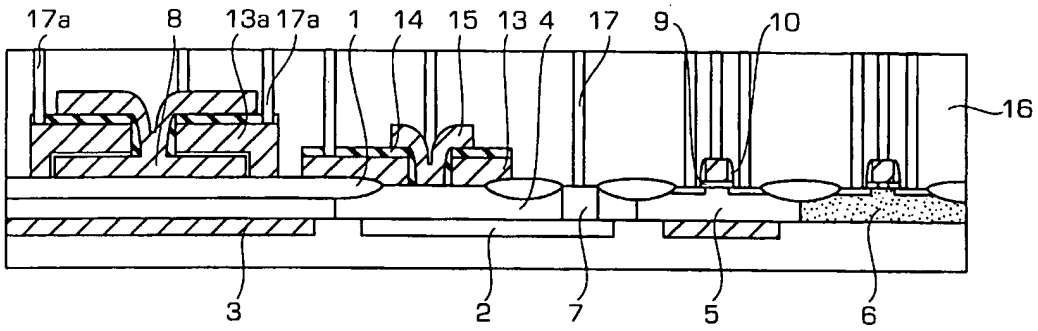
Figure 7 of the specification as originally filed is provided hereinbelow.

FIG. 7



Fujii - Figure 9 of Fujii is provided hereinbelow.

FIG. 9



Fujii arguably teaches the presence of a base electrode 13 and an emitter electrode 15 (Fujii at column 4, lines 37 and 39).

Fujii, at column 8, lines 27-30, provides that after this, as shown in FIG. 9, a *first interlayer insulating film 16* is formed over the entire surface, and *holes are made at required positions* and *filled up with polysilicon*, and thereby *first layer contacts 17* are formed.

However, the Office Action readily admits that Fujii fails to teach the holes being simultaneously formed (Office Action at page 4).

- ***Thus, Fujii fails to disclose, teach, or suggest forming base and emitter electrode lead openings within said insulating film, said base electrode lead opening being formed simultaneous with said emitter electrode lead opening.***

Whereas Fujii arguably teaches that *holes are made at required positions* and *filled up with polysilicon* (Fujii at 8, lines 28-29), the Office Action ***readily admits*** that Fujii ***fails*** to disclose, teach or suggest *polishing* the polysilicon to separate the contacts 17.

- ***Thus, Fujii fails to disclose, teach, or suggest polishing said conducting film to separate said base electrode lead portion from said emitter electrode lead portion.***

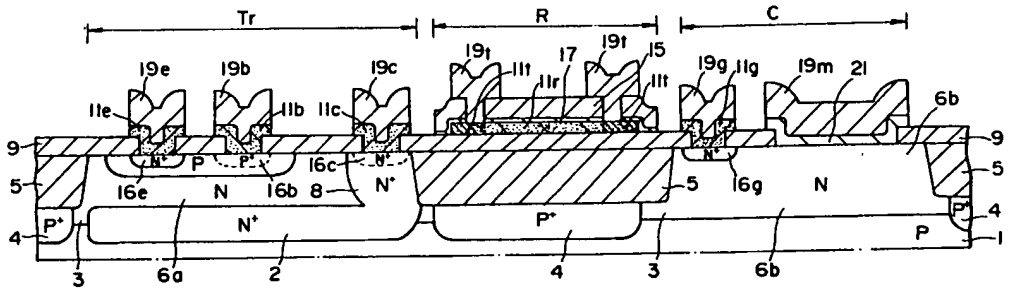
Fujii arguably teaches that in the first and the second embodiments described above, the first electrode of the ***capacitor*** and the ***gate electrodes*** of the MOSFETs are formed of polysilicon. However, the use of polycide that is *silicided* polysilicon with titanium, cobalt, molybdenum, tungsten or the like, is preferable, since it reduces the resistance value of the capacitor further down.

However, Fujii ***fails*** to teach a silicided base electrode lead portion or a silicided emitter electrode lead portion.

- ***Thus, Fujii fails to disclose, teach, or suggest depositing a silicide onto a polished surface of said conducting film.***

Horzumi - Figure 2M of Horzumi is provided hereinbelow.

FIG. 2M



Horzumi arguably teaches the presence of a base region 7.

However, the Office Action fails to show wherein there is to be found within Horzumi a step of forming the base region 7 on an insulator.

- ***Thus, the Office Action fails to show within Horzumi a step of forming a base layer on an insulator, said base layer being in contact with a portion of a semiconductor substrate.***

- ***Moreover, the Office Action fails to show that Horzumi teaches polishing said conducting film to separate said base electrode lead portion from said emitter electrode lead portion.***

In addition, the Office Action fails to show wherein there is to be found within Horzumi a silicided base electrode lead portion or a silicided emitter electrode lead portion.

- ***Thus, the Office Action fails to show that Horzumi teaches depositing a silicide onto a polished surface of said conducting film.***

Morimoto - Figures 2B-2C of Morimoto are provided hereinbelow.

Fig. 2B

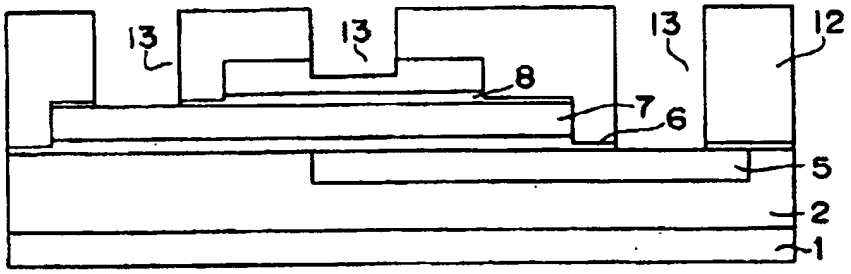
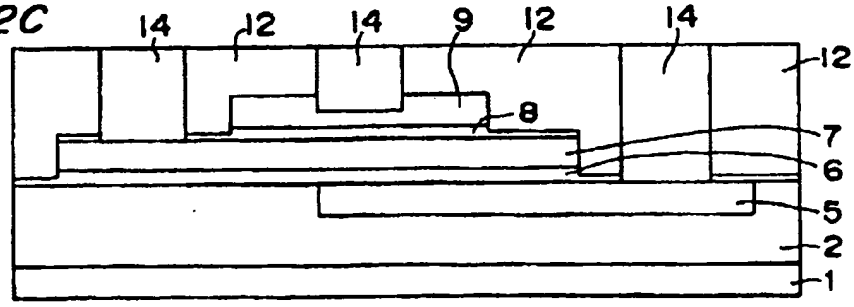


Fig. 2C



Morimoto arguably teaches that then, *surface polishing by the CMP method* is performed starting with the surface of the tungsten film 14 to *remove the tungsten and titanium nitride films* other than the film portions filled in the via holes, whereby a plug 14 (same reference number as that for the tungsten film is used for the sake of convenience) made of the titanium nitride film and the tungsten film 14 is formed in each via hole 13, as shown in FIG. 2C (Morimoto at column 6, lines 18-24).

Whereas the figures of Morimoto depict a capacitor, Morimoto ***fails*** to teach the presence of a bipolar transistor.

Additionally, Morimoto arguably teaches a tungsten plug 14 (Morimoto at column 6, line 19). However, Morimoto ***fails*** to teach a *silicided* plug 14.

- ***Thus, Morimoto fails to disclose, teach, or suggest depositing a silicide onto a polished surface of said conducting film.***

Besser - Figure 1 of Besser is provided hereinbelow.

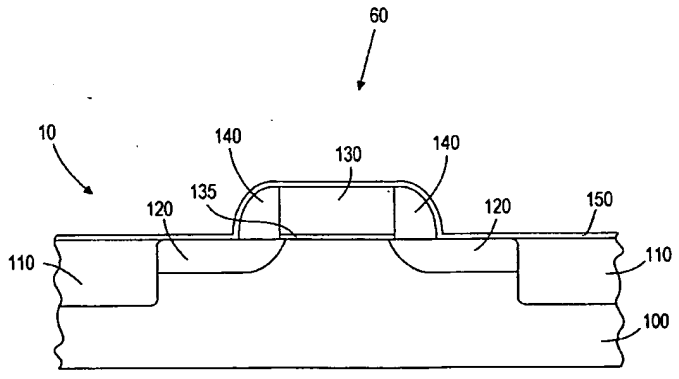


Fig. 1

Paragraph [0024] of Besser arguably teaches the following:

> [0024] A conventional *gate region 130* is formed on a gate oxide 135. Gate region 130 may comprise *doped polysilicon*. Spacers 140, which may be oxide spacers, are formed next to the sidewalls of gate region 130. A *metal layer 150* is deposited over the surface of wafer 10. According to an embodiment of the invention, metal layer 150 comprises nickel, although other metals may be used.

However, Besser fails to disclose, teach, or suggest gate region 130 being polished.

- ***Thus, Besser fails to disclose, teach, or suggest depositing a silicide onto a polished surface of said conducting film.***

Newly added claims

Claims 16-25 - Claims 17-25 are dependent upon claim 16. Claim 16 is drawn to a method for manufacturing a bipolar transistor, the method comprising the steps of:

> forming a base layer on an insulator, said base layer being in contact with a portion of a semiconductor substrate;
>
> forming an insulating film on said base layer;
>
> forming base and emitter electrode lead openings within said insulating film, said base electrode lead opening being formed simultaneous with said emitter electrode lead opening;
>
> depositing a conducting film into said base electrode lead opening and into said emitter electrode lead opening, said conducting film within said base electrode lead

opening being a base electrode lead portion and said conducting film within said emitter electrode lead opening being an emitter electrode lead portion; thereafter,

polishing said conducting film to separate said base electrode lead portion from said emitter electrode lead portion; and

forming a silicide on a polished surface of said conducting film.

Whereas claim 14 provides for the step of *"depositing a silicide onto a polished surface of said conducting film"*, claim 16 provides for the step of *"forming a silicide on a polished surface of said conducting film"*.

The step of "forming a silicide" is also absent from Fujii, Hozumi, Morimoto, and Besser, either individually or as a whole.

Allowance of the claims is respectfully requested.

Conclusion

For the foregoing reasons, all the claims now pending in the present application are allowable, and the present application is in condition for allowance. Therefore, this response is believed to be a complete response to the Office Action.

Applicants reserve the right to set forth further arguments supporting the patentability of their claims, including the separate patentability of the dependent claims not explicitly addressed herein, in future papers.

There is no concession as to the veracity of Official Notice, if taken in any Office Action. An affidavit or document should be provided in support of any Official Notice taken. 37 CFR 1.104(d)(2), MPEP § 2144.03. See also, *Ex parte Natale*, 11 USPQ2d 1222, 1227-1228 (Bd.

Pat. App. & Int. 1989)(failure to provide any objective evidence to support the challenged use of Official Notice constitutes clear and reversible error).

Accordingly, favorable reexamination and reconsideration of the application in light of the remarks is courteously solicited.

Extensions of time

Please treat any concurrent or future reply, requiring a petition for an extension of time under 37 C.F.R. §1.136, as incorporating a petition for extension of time for the appropriate length of time.

The Commissioner is hereby authorized to charge all required fees, fees under 37 C.F.R. §1.17, or all required extension of time fees. If any fee is required or any overpayment made, the Commissioner is hereby authorized to charge the fee or credit the overpayment to Deposit Account # 18-0013.

If the Examiner has any comments or suggestions that could place this application in even better form, the Examiner is requested to telephone Brian K. Dutton, Reg. No. 47,255, at 202-955-8753.

Dated: March 13, 2008

Respectfully submitted,

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